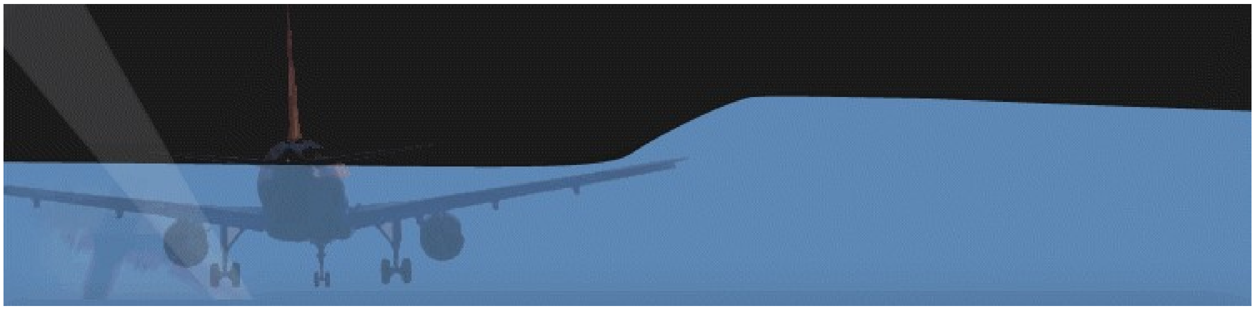

Plan for Hardware Aspects of Certification

for the

<Company Name> <Program Name>

Document No: <Doc Number>
Revision: -

____ ____________
<Name>, Program Manager Date

____ ____________
<Name>, Technical Project Lead Date

____ ____________
<Name>, Engineer Date

____ ____________
<Name>, Process Assurance Engineer Date

Notice

REVISIONS			
Rev.	Reason/Description	Requested/ Changed By	Date

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1.0 INTRODUCTION

This is a self-educating template. Note that blue italicized font is "Comment" text – it is instructional text used to educate the user of this template about DO-254 and how to use this template in terms of the intent or types of content required for a section. ***This text should be deleted once this template is turned into a real project document.*** Standard text *provides sample content (and/or example content) that can sometimes be used but must usually be customized for the specific project.*

This PHAC document summarizes the processes used to develop, design, verify and control the applicable hardware during the planning, development, verification, and production phases. References are made to the relevant planning, requirements, design, production, verification and configuration control documents and data. The purpose of this document is to communicate how the pertinent objectives of DO-254 and other certification criteria will be met and reviewed for FAA/EASA (or other) certification/approval.

You need to tailor the content of this PHAC based on the DAL of your project. Refer to Table 5-3. DO-254 Compliance Matrix" to help you do this.

Note that all the relevant figures in this template set are available for editing and provided in the free "drawio" format as part of this template set.

Also note that any place where there is a document name or "<doc-ref#>," ensure you replace these with the appropriate name/document reference as per your company standards.

1.1 Purpose

This Plan for Hardware Aspects of Certification (PHAC) defines the processes, procedures, methods, and standards to be used and the life cycle data to be produced to satisfy the objectives of DO-254 and any additional objectives required to satisfy the certification basis of the aircraft. Once approved, this PHAC represents an agreement between the applicant and the customer and/or certification authority.

1.2 Scope

Note that you can choose to create a PHAC for any level of hardware item (i.e., FPGA, board, etc.) and combine (or not) multiple hardware items into one plan. Just be very clear of the scope. Also note that Order 8110.105A and AMC 20-152A both clarify that it is no longer just "custom microcoded components" but also any digital or analog custom chips, boards, COTs, COTS IP, etc. that fall under the scope of DO-254.

This plan will be used by the customer and/or certification authority to determine if the Hardware Life Cycle Process is commensurate with the rigor required for the level of the hardware being developed. The hardware item described within the scope of this document is an FPGA *<or multiple FPGAs or other components, or board, or …>*. Once approved, it is implemented during the hardware life cycle development and supporting processes. This Plan for Hardware Aspects of Certification complies with the documentation requirements of RTCA/DO-254, Section 10.1.1.

1.3 Definitions

Modify this to include the terms used in your project.

The following table defines the key terms used in this project.

Table 1-1. Definitions

Definition	Meaning
COTS IP	As per AMC 20-152A: IP refers to design functions (design modules or functional blocks, including IP libraries) used to design and implement a part of or a complete custom device such as a PLD, FPGA, or ASIC. IP is considered to be commercial off-the-shelf intellectual property, i.e. 'COTS IP', when it is a commercially available function, used by a number of different users, in a variety of applications and installations.
<Term 2>	*<definition>*
<Term 3>	*<definition>*
<Term 4>	*<definition>*

1.4 Part Number and Nomenclature

Update with your own PN and nomenclature information.
This section includes the Part Number(s) of the AEH device covered by this PHAC.

Table 1-2. Part Number and Nomenclature

Part Number	Nomenclature
PC-XY-1234-56_FH	Flight Hardware
<next applicable PN>	*<PN Description>*

1.5 Deviations

DO-254 acknowledges that from time to time you will want to deviate from the agreed to and approved plans. When this happens a defined method for how these deviations will be communicated and agreed should be defined. This section provides an example concept for how a company could chose to do this. Modify this section with the method you determine best suited for your company.

Deviations to this plan once it is approved will be documented in problem reports (PRs) against this PHAC or any other lower level affected plan or standards document. Deviation PRs will be communicated to the authority responsible for approving the deviation. This PR will contain the "is" and "was" changes for the deviation to the plan, standard, or process. Deviations that are deemed "significant" will result in an update to this plan and a resubmittal for approval. Significant changes to plans are those that affect tool qualification, design and verification methodologies, and life cycles such that a different methodology is used.

1.6 Team Members & Organization

List all team members involved in the project, identifying those with signature authority, and provide an organization structure demonstrating independence among the pertinent functions. The text provided describes the typical job descriptions and responsibilities but should be updated to reflect those in your organization who are involved in your program.

The Organization Chart shown in Figure 1-1 depicts the high-level organization involved in this program.

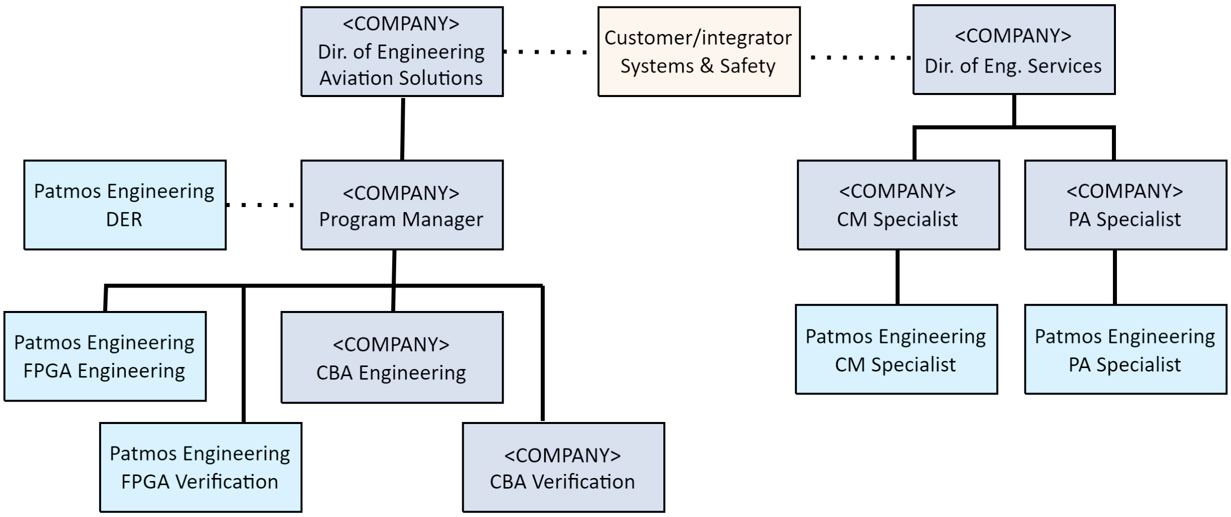
<COMPANY> Dir. of Engineering Aviation Solutions
Customer/integrator Systems & Safety
<COMPANY> Dir. of Eng. Services
Patmos Engineering DER
<COMPANY> Program Manager
<COMPANY> CM Specialist
<COMPANY> PA Specialist
Patmos Engineering FPGA Engineering
<COMPANY> CBA Engineering
Patmos Engineering CM Specialist
Patmos Engineering PA Specialist
Patmos Engineering FPGA Verification
<COMPANY> CBA Verification

Figure 1-1. Program Organization Chart

The scope of this project is an FPGA, which is a component of a larger hardware project involving a circuit board assembly (CBA). The project team for the FPGA will communicate and work with the CBA team as needed. The FPGA engineering, verification, Process Assurance, and Configuration Management is being handled by a sub-contractor (Patmos Engineering Services). See Section 5.4.12 for more information on the proper oversite of this subcontractor.

The following table identifies the team members and their roles. The subsections that follow describe the roles in detail.

Table 1-3. Team Members and Signature Authority

Name	Title
Signature Authority:	
<NAME>	Program Manager
<NAME>	Lead FPGA Hardware Engineer
<NAME>	Independent FPGA Verification Engineer
<NAME>	Process Assurance Engineer
Team Members:	
<NAME>	Systems Engineer
<NAME>	Reliability & Safety Engineer
<NAME>	Hardware CBA Design Engineer
<NAME>	Configuration Management Engineer

<NAME>	Certification Authority / Certification Representative / FAA Hardware Designated Engineering Representative

Assigned project personnel will perform the various activities identified in this plan. Key individuals are responsible for tasks assigned based on their respective area of expertise. These include Program Management, Hardware Engineering, Hardware Verification, Hardware Configuration Management, and Hardware Process Assurance. Peer Reviews will be used for all Hardware verification process activities requiring independence.

1.6.1 Program Manager

The Program Manager will support preparation and implementation of various planning, requirements, and design descriptions for the project. Responsibilities include, but are not limited to, the following:

- Chairing the Engineering Review
- Developing and maintaining the project schedule
- Managing all development activities
- Assigning personnel and priorities
- Ensuring readiness for scheduled project reviews
- Resolving all process- and product-related problems/concerns
- Ensuring that the necessary equipment and tools are available for development

1.6.2 Hardware Engineering

The Hardware Engineer supports the following tasks:

- Participate in Hardware requirements reviews.
- Participate in Hardware architectural design reviews.
- Participate in code reviews.
- Participate in integration reviews.
- Process Hardware Problem Reports, Change Requests, and Initial Baseline Items.
- Develop and maintain all trace matrices involving requirements, design, and code.
- Provide support for test case and procedure preparation.
- Support elemental analysis.
- Support requirements coverage analysis.

1.6.3 Independent Verification and Validation (V&V)

The Independent V&V Engineer supports the following tasks:

- Participate in Hardware requirements reviews.
- Participate in Hardware architectural design reviews.
- Participate in code reviews.
- Participate in integration reviews.
- Process Hardware Problem Reports, Change Requests, and Initial Baseline Items.
- Verify all trace matrices involving requirements, design, and code.
- Create test cases and procedures.
- Execute test cases.
- Perform elemental analysis.
- Perform requirements coverage analysis.

1.6.4 Hardware Configuration Management

The hardware Configuration Management (CM) Engineer will ensure configuration control of all hardware and environmental items, as well as documentation, produced or used within the scope of this program. Details of the CM activities are identified in the Hardware Configuration Management Plan (HCMP), <COMPANY> document <doc-ref#>_HCMP.

In summary, the Hardware CM Engineer performs the following tasks:

- Problem Reporting System Setup, Maintenance and Reporting: Administer and maintain the PRs.
- Configuration Management Hardware Library Setup, Maintenance, and Reporting: Setup, configuration, and maintenance of the code management tool.
- Revision Control: Ensures that all product releases are reproducible, versioned, dated, and archived.
- Hardware Configuration Index Preparation: Ensures that a configuration index is created for the certifiable configuration.
- Hardware Environment Configuration Index Preparation: Ensures that an HECI is created for the certifiable configuration.
- Data Configuration: Configures the Hardware life-cycle data generated during development and qualification.
- Tool and Release Archival: Performs backup and archival of all Hardware life-cycle data.
- Release Builds: Builds release configuration for test and final release.
- Archiving and safeguarding the production configuration.
- Media recreation to ensure ability to reproduce the development and verification environments, as well as the object code.
- Independent builds of released configuration for verification testing and production.
- Loading the Hardware configuration into production hardware.

Note that in the scope of this project, this role is performed by the subcontractor, who reports directly to the <COMPANY> corporate configuration management specialist.

1.6.5 Hardware Process Assurance

The hardware Process Assurance (PA) Engineer will provide independent review of all verification activities and has review responsibility for related objective evidence. Throughout the development life cycle, the Process Assurance Engineer will conduct and/or participate in all project reviews and audits. Details of the PA activities are identified in the Hardware Process Assurance Plan (HPAP), <COMPANY> document <doc-ref#>_HPAP.

In summary, the hardware Process Assurance is responsible for the following activities:

- Approve Hardware life cycle data for transition through the development phases.
- Audits verification activities per the HPAP. The audits will include:
  - verification test witnessing
  - spot-checking of the verification environment
  - spot-checking the outputs of the verification activities
- Verifies that no conflicts exist between plans and standards.
- Participate in high-level requirements reviews and Hardware design reviews.
- Participate in code reviews as needed.
- Conduct reviews of the outputs of the Integration and Test phase.

- Conduct reviews of the test cases, procedures, and results.
- Create Hardware problem reports and validate disposition.
- Maintain all trace matrices involving testing.
- Functional Analysis – Hardware Integration Analysis
- Verify Configuration Control

To provide greater robustness of the Hardware, additional verification activities may be reviewed / witnessed by the Process Assurance Engineer as explained in the Hardware Verification Plan (HVVP), <doc-ref#>_HVVP.

Note that in the scope of this project, this role is performed by the subcontractor, who reports directly to the <COMPANY> corporate Process/Quality Assurance specialist.

1.6.5.1 Organizational Independence

The Org Chart of Figure 1-1 shows that the Process Assurance Organization is independent from Engineering. It also demonstrates that the verification and test activities are performed independently by someone other than the development engineer.

1.6.6 FAA Hardware Designated Engineering Representative

A Designated Engineering Representative (DER) will be employed to perform reviews and audits to find compliance with applicable 14 CFR's (where the FAA has delegated authority). The Hardware DER's role on this project is summarized below:

- Ensures there is tangible evidence to show that the objectives of DO-254, other applicable guidance, issue papers, and so forth are satisfied.
- Approves or recommends approval of Hardware plans, data, and compliance findings by issuing 8110-3 forms against regulations.
- Ensures that the processes established are yielding the results desired – i.e., making sure the development, verification, or integral processes are allowing the teams to satisfy the DO-254 objectives.
- Works closely with Hardware Process Assurance to ensure that processes and plans are being followed.
- Follows FAA Orders and other applicable FAA policy documents related to the designee system.
- Ensures that all open problem reports (OPRs) have been evaluated to not negatively impact safety prior to certification.
- Performs routine reviews on projects that he/she will be approving.
- Documents the review results in writing.
- Uses the FAA Hardware Review Job Aid (or other applicable document) to assist in conducting reviews.
- Informs the FAA when reviews are planned and encourages FAA involvement.
- Ensures that the project team addresses review findings/observations.
- Ensures that the ongoing verification process with project-level peers is being carried out properly.
- Prepares the development team for reviews by other designees or the FAA.

1.6.7 Signature Authority Explained

“Signature Authority”, as used herein, is a project-level approval authority that is composed of the following members at minimum:

- Program Manager
- Hardware Lead
- Independent Verification Engineer
- Hardware Process Assurance/Quality Engineer

Other team members may be required to sign specific documents in addition to this core group, depending on the content of the document. For example, a Configuration Management Specialist is required to sign the Configuration Management Plan to acknowledge acceptance of the CM processes defined therein.

1.7 Acronyms and Abbreviations

Add any of your own Acronyms that are pertinent.

AEH	Airborne Electronic Hardware
ALU	Arithmetic Logic Unit
ARP	Aerospace Recommended Practice
ASIC	Application Specific Integrated Circuit
CBA	Circuit Board Assembly
CD	Custom Device
CEH	Complex Electronic Hardware
CFR	Code of Federal Regulations
COTS	Commercial-Off-The-Shelf
CPLD	Complex Programmable Logic Device
EASA	European Aviation Safety Agency
EUROCAE	European Organization for Civil Aviation Equipment
FFP	Functional Failure Path
FFPA	Functional Failure Path Analysis
FHA	Functional Hazard Assessment
FMEA	Failure Modes and Effects Analysis
FTA	Fault Tree Analysis
HAS	Hardware Accomplishment Summary
HC1	Hardware Control Category 1
HC2	Hardware Control Category 2
HCI	Hardware Configuration Index
HCM	Hardware Configuration Management
HDD	Hardware Design Document
HDL	Hardware Description Language
HECI	Hardware Environment Configuration Index
IP	Intellectual Property, or Issue Paper
LRU	Line Replaceable Unit
PA	(Hardware) Process Assurance
PCB	Printed Circuit Board
PHAC	Plan for Hardware Aspects of Certification
PLD	Programmable Logic Device
PSSA	Preliminary System Safety Assessment
SAE	Society of Automotive Engineers
SC	Special Committee
SEH	Simple Electronic Hardware
SSA	System Safety Assessment